REMARKS

Claims 1-19 are pending. Claims 1-10, 12, and 16 are being amended to clarify the invention. Claim 19 has been added. No new matter has been added by way of this amendment.

Information Disclosure Statement

The Examiner has indicated he has not considered "Improving Binary Compatibility in VLIW Machines Through Compiler Assisted Dynamic Rescheduling" by Biglari-Abhari, M. et al. ("Biglari-Abhari") because a copy of the reference is not in the application. Applicants note that the Biglari-Abhari reference is contained in the application but was incorrectly entered in the Image File Wrapper ("IFW"). The reference is contained behind EP 1 152 329 A1 at pages 18-25 of that reference in the IFW. Nevertheless, Applicants have submitted a new copy of the reference in the Supplemental Information Disclosure Statement dated February 16, 2007.

Oath/Declaration/Application Data Sheet

The Examiner has indicated that a new oath, declaration, or Application Data Sheet is required because the certified priority document does not correspond to the identified priority document. Enclosed is a Supplemental Application Data Sheet that corresponds to the certified priority document. Applicants have concurrently filed a Petition to Accept Late Priority Claim Under 37 C.F.R. § 1.55(c).

The Examiner has also indicated that a new oath or declaration is needed because the clause regarding "willful false statements" has been omitted. Enclosed is a new declaration including a clause regarding "willful false statements" signed by the inventors.

Indefiniteness

The Examiner has rejected claims 1-11 and 16-18 under 35 U.S.C. § 112, ¶ 2 as being indefinite for failing to particular point out and distinctly claim the invention. With respect to claim 1, the Examiner has indicated that the claim recites numerous examples of "said order," which are not clear. Dependent claims 2-11, which depend on claim 1, inherit this rejection.

Applicants have amended claim 1 to recite "an order" and changed the "ordering" step to a "separating" step, thus clarifying the phrase "said order." Accordingly, Applicants request that the Examiner withdraw his rejection.

The Examiner has indicated that it is unclear in claim 4 what "one" refers to in the phrase "detecting when one between". Applicants have amended claim 4 to remove the unclear phrase. Accordingly, Applicants request that the Examiner withdraw his rejection.

The Examiner has also indicated that there is no antecedent basis for "said instruction stream" in claim 16. Dependent claims 17 and 18, which depend on claim 16, inherit this rejection. Applicants have amended claim 16 to recite "an instruction stream." Accordingly, Applicants request that the Examiner withdraw his rejection.

Menezes Does Not Anticipate Claims 1-18

The Examiner has rejected claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,950,926 issued to Menezes ('Menezes").

Menezes discloses a method for determining dependencies in a group of instructions executed in a microprocessor. In particular, the disclosed method includes fetching both instructions and associated dependency instructions from storage. The dependency instructions, for example, are inserted in neutral instructions, which do not change the machine state. In one embodiment, the dependencies are defined among single instructions. Menezes 4:15-27, 4:63 and 5:6. In addition, in some embodiments, Menezes also discloses there can be a relationship among a set of instructions. Menezes 5:59 – 6:15. Thus, a first set and a second set can have internal dependencies within a set as well as dependencies between the instruction sets.

Claim 1, as amended, recites the step of "separating said bundles of instructions into respective sub-bundles, said sub-bundles identifying a first set of instructions, *which must be executed before the instructions belonging to the next bundle* of said order, and a second set of instructions that *can be executed both before and in parallel with respect to the instructions belonging to said next bundle* of said order, it being possible for at least said second set of instructions to be the null set." (emphasis added). Thus, groups of instructions are further separated into two sub-bundles. The first sub-bundle contains a set of instructions that must

execute before any instructions belonging to the subsequent group and a second sub-bundle containing a set of instructions that may be executed in parallel with the subsequent group.

Menezes does not disclose the invention as recited in claim 1. Specifically, Menezes does not teach the recited "separating" step. Menezes does not teach further separating a set of instructions other than on the internal dependency of the instructions in the set. However, as recited in claim 1, each bundle is separated into two sub-bundles based on whether the instructions must be executed before the instructions of the next set, *not the current set*. In addition, Menezes does not teach the recited "can" sub-bundle which may be executed in parallel with instructions of the next bundle. In Menezes, when *any* instruction in the second set depends on an instruction in the first set, the issue of the second set is either stalled until the first set completes or hardware dependency checking circuitry can examine the instruction stream to decide how the second set should be issued. Menezes 6:12-13 (emphasis added). If the second set is stalled until the first set completes, it cannot execute in parallel with respect to the instructions of the first set. If the hardware dependency circuitry examines the instruction stream to decide how the second set should be issued, it does not determine what instructions of the first set can be executed in parallel with the second set.

Accordingly, for at least these reasons, there is no anticipation of claim 1, or claims 2-11, which depend on claim 1.

In addition, claims 3-4 and 5 recite identifying the instructions belonging to a sub-bundle of said first set and of said second set by means of a binary symbol or two distinct binary symbols, respectively. Menezes does not teach, suggest, or motivate the use of a binary symbol or two binary symbols to identify the instructions belonging to a sub-bundle. Menezes specifically requires the introduction of an additional instruction to supply dependency information. Menezes 4:29-62; 6:50-62. Since a neutral instruction or a new dependency instruction as described in Menezes is more than two binary symbols, Menezes fails to anticipate claims 3-5. Accordingly, claims 3-5 are also allowable over Menezes for at least this additional reason.

Menezes does not disclose the invention recited in claim 12. Claim 12, as amended, recites, "providing in each encoded instruction a designated number of initial bits

identifying said predetermined priority of the instruction set." Menezes does not teach using a designated number of initial bits in each encoded instruction. As previously stated, Menezes requires the introduction of an additional instruction to supply dependency information. Menezes 4:29-62; 6:50-62. Therefore, Menezes does not disclose that each encoded instruction has a designated number of initial bits identifying said predetermined priority of the instruction set.

Accordingly, for at least these reasons, there is no anticipation of claim 12, or claims 13-15 and 19, which depend on claim 12.

Although the language of claims 16-18 is not identical to that of claim 12, the allowability of those claims will be apparent in view of the above remarks.

Conclusion

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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Enclosure:
Supplemental Application Data Sheet
New Declaration and Power of Attorney

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